

SE (EXTC) SEM: III (CBCSGs) NOV-DEC 2013

Digital Electronics
4/12/13

GX-12122

16 : 2nd half.13-Avi(at)

Con. 8622-13.

(3 Hours)

[Total Marks : 80

- N.B. : (1) Question No. 1 is compulsory.
 (2) Out of remaining questions, attempt any three questions.
 (3) Assume suitable additional data if required.
 (4) Figures in brackets on the right hand side indicate full marks.

1.	(A) Compare combinational circuits with sequential circuits. (05) (B) Compare TTL with CMOS logic families. (05) (C) Compare SRAM with DRAM. (05) (D) Compare FPGAs with CPLDs. (05)
2.	(A) State and prove De Morgan's theorem. (10) (B) Using Quine McClusky method, minimize the following: $F(A, B, C, D) = \sum_{E} m(0, 1, 3, 7, 8, 9, 11, 15, 22, 24, 27) + d(6, 16).$ (10)
3.	(A) Implement the following Boolean equation using single 8:1 MUX and few logic gates: $F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15).$ (10) (B) Write $(32)_{10}$ into its BCD code, and Ex-3 code. (05) (C) Implement $Y = A + \overline{BC}$ using only NOR gates. (05)
4.	(A) Draw a neat circuit of BCD adder using IC 7483 and explain. (10) (B) It is desired to develop the circuit for controlling a lamp on a staircase between 1 st and 2 nd floor of a building. Each floor is having only one switch. If a lamp is made 'ON' using switch of 1 st floor, one should be able to switch it 'OFF' using a switch of 2 nd floor and vice-versa. Design the circuit for the same. Write the VHDL code for the same. (10)
5.	(A) What is shift register? Explain any one type of shift register. Give its application. (10) (B) Convert D type flip flop into T type flip flop. (05) (C) Compare PAL with PLA. (05)
6.	(A) Design a synchronous counter using D type flip flops for getting the following sequence: 0 - 2 - 4 - 6 - 0. Take care of lockout condition. (10) (B) Explain any one application of Johnson counter. (05) (C) Draw the block diagram of internal architecture of XC9500 family CPLD and explain in brief. (05)